AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Currently amended) An electrophoretic display comprising:

a first gate line and a second gate line which extend in a first direction;

a first data line and a second data line which extend in a second direction substantially perpendicular to the first direction; [[and]]

a first pixel electrode disposed in a first region restricted by the first gate line, the second gate line, the first data line and the second data line; and

a thin-film transistor comprising:

a source electrode connected to the first data line;

a gate electrode connected to the first gate line; and

a drain electrode connected to the first pixel electrode,

wherein

entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line, respectively, and

the first pixel electrode covers only the drain electrode of the thin-film transistor.

2. (Previously presented) The electrophoretic display of claim 1, further comprising a second pixel electrode disposed in a second region adjacent to the first region, wherein

the second pixel electrode comprises a first side and a second side opposite the first side, and

one of the first data line and the second data line overlaps an entire length of an edge of the second pixel electrode defining one of the first side of the second pixel electrode and the second side of the second pixel electrode.

3. (Previously presented) The electrophoretic display of claim 1, further comprising:

an insulating layer interposed between one of the first data line and the second data line and the first pixel electrode,

wherein the insulating layer has a dielectric constant lower than approximately 4.

4. (Previously presented) The electrophoretic display of claim 1, wherein one of the first data line and the second data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti.

5. (Canceled)

6. (Previously presented) The electrophoretic display of claim 3, wherein the insulating layer is made of one of a-Si:C:O and a-Si:O:F.

7. (Currently amended) An electrophoretic display comprising:

a substrate;

a first gate line and a second gate line which extend in a first direction; and

a first data line and a second data line which extend in a second direction substantially perpendicular to the first direction;

a first thin film transistor comprising:

a first channel;

a first gate electrode;

a first source electrode;

a first drain electrode; and

a first semiconductor layer;

a first opaque layer formed on the first semiconductor layer and disposed over the channel of the first thin film transistor;

a second thin film transistor disposed adjacent to the first thin film transistor and comprising:

a second channel;

a second gate electrode;

a second source electrode;

a second drain electrode; and

a second semiconductor layer;

a second opaque layer formed on the second semiconductor layer and disposed over the channel of the second thin film transistor;

a first pixel electrode disposed over only the first drain electrode of the first thin film transistor; and

a second pixel electrode disposed over the second thin film transistor,

wherein entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line, respectively.

8. (Canceled)

9. (Previously presented) The electrophoretic display of claim 7, further comprising:

an insulating layer formed between the one of the first data line and the second data line and one of the first pixel electrode and the second pixel electrode,

wherein the insulating layer has a dielectric constant smaller than approximately 4.

10. (Previously presented) The electrophoretic display of claim 7, wherein one of the first data line and the second data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti.

11. (Canceled)

12. (Previously presented) The electrophoretic display of claim 9, wherein the insulating layer is made of one of a-Si:C:O and a-Si:O:F.

13. (Canceled)

14. (Currently amended) An electrophoretic display comprising:

a substrate;

a thin film transistor formed on a surface of the substrate, the thin film transistor comprising:

a source electrode and a drain electrode formed on the substrate;

a semiconductor layer formed on the source electrode and the drain electrode;

an insulation layer formed on the semiconductor layer; and

a gate electrode formed on the insulation layer;

a first gate line and a second gate line which extend in a first direction;

a first data line and a second data line which extend in a second direction substantially perpendicular to the first direction;

a first pixel electrode disposed in a first region restricted by the first gate line, the second gate line, the first data line and the second data line; and

a second pixel electrode disposed in a second region adjacent to the first region,

wherein entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line, and

the first pixel electrode covers only the drain electrode of the thin-film transistor.

15. (Canceled)

16. (Previously presented) The electrophoretic display of claim 14, further comprising:

an insulating layer formed between one of the first data line and the second data line and one of the first pixel electrode and the second pixel electrode,

wherein the insulating layer has a dielectric constant smaller than approximately 4.

17. (Previously presented) The electrophoretic display of claim 14,

wherein one of the first data line and the second data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti.

18. (Previously presented) The electrophoretic display of claim 14, wherein an inclination angle of one of the first gate line, the second date line, the first data line and the second data line

relative to a surface of the substrate ranges from between approximately 20 degrees to approximately 80 degrees.

19. (Previously presented) The electrophoretic display of claim 16, wherein the insulating layer is made of one of a-Si:C:O and a-Si:O:F.

20. (Currently amended) An electrophoretic display comprising:

a first gate line and a second gate line which extend in a first direction;

a first data line and a second data line which extend in a second direction substantially perpendicular to the first direction;

a first pixel electrode disposed in a first region restricted by the first gate line, the second gate line, the first data line and the second data line;

a second pixel electrode disposed in a second region adjacent to the first region;

a common electrode; [[and]]

a plurality of micro-capsules; and

a thin-film transistor comprising:

a source electrode connected to the first data line;

a gate electrode connected to the first gate line; and

a drain electrode connected to the first pixel electrode, wherein

each microcapsule of the plurality of microcapsules comprises electric ink comprising a plurality of color pigment particles, ~~wherein~~

a color of the plurality of color pigment particles is at least one of red, green, blue, cyan, yellow, magenta, black and white, [[and]]

entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line, and

the first pixel electrode covers only the drain electrode of the thin-film transistor.

21. (Previously presented) The electrophoretic display of claim 20, wherein the second pixel electrode comprises a first side and a second side opposite the first side, and

one of the first data line and the second data line overlaps an entire length of an edge of the second pixel electrode defining one of the first side of the second pixel electrode and the second side of the second pixel electrode.

22. (Previously presented) The electrophoretic display of claim 20, further comprising:

an insulating layer formed between one of the first data line and the second data line and one of the first pixel electrode and the second pixel electrode,

wherein the insulating layer has a dielectric constant lower approximately 4.

23. (Canceled)

24. (Previously presented) The electrophoretic display of claim 1, wherein entire lengths of opposing edges of the first pixel electrode defining a third side and a fourth side of the first pixel electrode along the first direction between the first data line and the second data line overlap the first gate line and the second gate line, respectively.

25. (Previously presented) The electrophoretic display of claim 7, wherein entire lengths of opposing edges of the first pixel electrode defining a third side and a fourth side of the first pixel electrode along the first direction between the first data line and the second data line overlap the first gate line and the second gate line, respectively.

26. (Previously presented) The electrophoretic display of claim 14, wherein entire lengths of opposing edges of the first pixel electrode defining a third side and a fourth side of the first pixel electrode along the first direction between the first data line and the second data line overlap the first gate line and the second gate line, respectively.

27. (Previously presented) The electrophoretic display of claim 20, wherein entire lengths of opposing edges of the first pixel electrode defining a third side and a fourth side of the first pixel electrode along the first direction between the first data line and the second data line overlap the first gate line and the second gate line, respectively.